IN THE CLAIMS:

Cancel claims 40, 41, 42, 43, 54, and 55.

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

32. (Two Times Amended) A method for forming a high density multi-chip module, comprising:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die of said plurality having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;

forming a pattern of a plurality of electrical conductors associated with said substrate one each said first side and second side of said substrate, at least one electrical conductor of said plurality of electrical conductors having a connection terminal adjacent a through-slot of said at least three through-slots for connecting said plurality of bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

connecting said conductor pattern on said first side and said second side of said substrate with conductive vias through said substrate;

forming an input/output connector on said substrate and connecting said input/output connector to said plurality of electrical conductors, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said plurality of semiconductor dice;

attaching the active surfaces of a plurality of said plurality of semiconductor dice to the first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the plurality of bond pads of said at least one semiconductor die aligned with other alternate through-slots of said at least three through-slots for access from the first side of said substrate; and

wire-bonding said plurality of bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the alternate through-slots.

33. (Previously Amended) The method of claim 32, wherein forming through-slots comprises forming an elongate stepped surface in said through-slots.

34. (Two Times Amended) The method of claim 33, wherein forming a pattern of electrical conductors includes forming conductive connection terminals on said elongate stepped surface.

35. (Two Times Amended) The method of claim 32, further comprising:

inserting a flowable hardenable glob-top material into each said through-slot to encapsulate wires therein.

36. (Previously Amended) The method of claim 35, wherein a hardenable polymeric material is inserted into each said through-slot.

37. (Previously Amended) The method of claim 35, wherein said glob-top material is inserted to extend outwardly between edges of at least two semiconductor dice of said plurality of semiconductor dice proximate each side of each said through-slot.

38. (Amended) The method of claim 32, further comprising:

performing electrical testing of said plurality of semiconductor dice following wire-bonding thereof and prior to wire encapsulation.

39. (Two Times Amended) The method of claim 32, further comprising:

encapsulating said plurality of dice with a polymeric sealant.

44. (Two Times Amended) A method for forming a high density multi-chip module, comprising:

providing a plurality of integrated circuit dice, each die of said plurality having an active surface with a row of conductive bond pads thereon;

forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;

forming a pattern of electrical conductors associated with said substrate and having connection terminals adjacent each of said at least three through-slots for connecting said bond pads to an input/output connector;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said bond pads, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice;

attaching the active surfaces of a plurality of said plurality of integrated circuit dice to said first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one of said plurality of dice to said second side of said substrate wherein the bond pads thereof are aligned with other alternate through-slots for access from the first side of said substrate; and

wire-bonding said bond pads of each attached die to connection terminals adjacent the corresponding through-slot.

45. (Previously Amended) The method of claim 44, wherein forming through-slots comprises forming an elongate stepped surface in each said through-slot.

46. (Two Times Amended) The method of claim 45, wherein forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

47. (Two Times Amended) The method of claim 44, further comprising inserting a flowable hardenable glob-top material into each said through-slot to encapsulate wires therein.

48. (Previously Amended) The method of claim 47, wherein a hardenable polymeric material is inserted into each said through-slot.

49. (Previously Amended) The method of claim 47, wherein said glob-top material is inserted to extend outwardly between edges of dice proximate each side of each said through-slot.

50. (Amended) The method of claim 44, further comprising:
performing electrical testing of said dice following wire-bonding thereof and prior to wire encapsulation.

51. (Two Times Amended) The method of claim 44, further comprising:
encapsulating said dice with a polymeric sealant.

52. (Two Times Amended) The method of claim 44, wherein forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first and second sides of said substrate.

53. (Amended) The method of claim 52, further comprising:
connecting said two conductor patterns with conductive vias through said substrate.